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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,263	04/26/2004	Tung-Sheng Chen	13043-US-PA	3262

31561 7590 09/14/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,263	CHEN ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,8,11-15 and 23-25* is/are rejected.

7)☒ Claim(s) *4,5,7,9,10 and 16-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: NON-VOLATILE MEMORY CELL WITH GRADED CHARGE TRAPPING LAYER.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6, 8, 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hijiya et al.. As to claim 1, Hijiya et al., Figure 1, discloses a non-volatile memory cell comprising a tunnel dielectric layer (6) (col. 2, line 61) disposed on a substrate (1), a barrier dielectric layer (8) (col. 2, lines 62-63) disposed over the tunnel dielectric layer, a graded charge trapping layer, embodied as the interface between the tunnel dielectric layer (6) and the floating gate (7), disposed between the barrier dielectric layer (8) and the tunnel dielectric layer (6), wherein the compositional ratio of the graded charge trapping layer varies from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer (col. 3, lines 31-34), a gate conductive layer (9) (col. 2, line 64) disposed on the barrier dielectric layer, a source region (3) and a drain region (4) respectively disposed in the substrate along both sides of the gate conductive layer.

As to claim 2, Hijiya et al. (col. 3, lines 34-47) discloses that the compositional ratio of the graded charge trapping layer gradually decreases from one side of the graded charge trapping layer adjacent to

the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer. Since the graded layer is nitride near the substrate and oxide near the floating gate, the compositional ratio, which may be defined by the nitrogen-to-oxygen stoichiometric ratio, decreases in a manner within the scope of claim 2.

As to claim 3, Hijiya et al. (col. 3, lines 34-47) discloses that the compositional ratio of the graded charge trapping layer gradually increases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer. Since the graded layer is nitride near the substrate and oxide near the floating gate, the compositional ratio, which may be defined by the oxygen-to-nitrogen stoichiometric ratio, increases in a manner within the scope of claim 3.

As to claim 6, Hijiya et al. (col. 3, lines 34-47) discloses that the graded charge trapping layer (6) is a graded silicon nitride layer.

As to claim 8, Hijiya et al. (col. 3, lines 34-47) discloses that the silicon/nitrogen ratio of the graded charge trapping layer gradually increases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

As to claim 11, Hijiya et al. discloses (col. 3, lines 26-27) that the material of the tunnel dielectric layer (6) includes silicon oxide.

As to claim 12, Hijiya et al. discloses (col. 2, line 63) that the material of the barrier dielectric layer (8) includes silicon dioxide.

Claims 13-15 and 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Hijiya et al.. As to claim 13, Hijiya et al., Figure 6, discloses a non-volatile memory cell comprising a tunnel dielectric layer (6') (col. 5, line 13) disposed on a substrate (1), a barrier dielectric layer (8') (col. 5, line 13) disposed over the tunnel dielectric layer, a graded charge trapping layer, embodied as the interface between the tunnel dielectric layer (6') and the barrier dielectric layer (8'), disposed between the barrier dielectric layer (8') and the tunnel dielectric layer (6'), wherein the graded charge trapping layer has a graded band gap and the graded band gap comprises a plurality of trapping levels (shown as Figure 7A,

element 7'), a gate conductive layer (9) (col. 2, line 64) disposed on the barrier dielectric layer, a source region (3) and a drain region (4) respectively disposed in the substrate along both sides of the gate conductive layer.

As to claim 14, Hijiya et al., Figure 7A, discloses that the graded band gap of the graded charge trapping layer (7') gradually decreases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

As to claim 15, Hijiya et al., Figure 7B, discloses that the graded band gap of the graded charge trapping layer (7') gradually increases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

As to claim 23, Hijiya et al. discloses (col. 5, lines 25-27) that the material of the tunnel dielectric layer (6') includes silicon oxide.

As to claim 24, Hijiya et al. discloses (col. 5, line 13) that the material of the barrier dielectric layer (8') includes silicon dioxide. Hijiya et al. teaches (col. 5, line 12) that the dielectric layers (6') and (8') are dissimilar, but Hijiya et al. also teaches that dielectric layer (8') is insulating, analogously to dielectric layer (8), and is therefore within the scope of claim 24.

As to claim 25, Hijiya et al. (col. 3, lines 34-47) discloses that the graded charge trapping layer (6) is a graded silicon nitride layer, and that the tunnel dielectric layer (6'), which contains the charge trapping layer is manufactured in the same way as layer (6)(col. 5, lines 25-27).

Allowable Subject Matter

Claims 4, 5, 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the compositional ratio, or the specific silicon/nitrogen ratio of a graded charge trapping layer in the claimed invention that first gradually increases, then gradually decreases, or first gradually decreases, then gradually increases.

Claims 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses a graded silicon nitride layer in which the silicon/nitrogen ratio of the graded charge trapping layer gradually decreases from the side adjacent the tunnel dielectric layer to the side adjacent the barrier dielectric layer.

Claims 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the graded band gap of the graded charge trapping layer in the claimed invention that first gradually increases, then gradually decreases, or first gradually decreases, then gradually increases.

Claims 18-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with a number of trapping levels which varies from one side adjacent the tunnel dielectric layer to the other side adjacent the barrier dielectric layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
September 1, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800